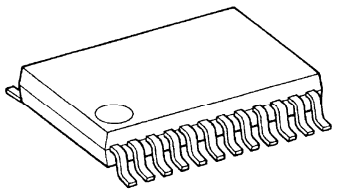
TOSHIBA Bi-CD Integrated Circuit Silicon Monolithic

TB6633FNG

3-Phase Full-Wave PWM Driver for Sensorless DC Motors

The TB6633FNG is a three-phase full-wave PWM driver for sensorless brushless DC (BLDC) motors. It controls motor rotation speed by changing the PWM duty cycle, based on the voltage of an analo control input.



SSOP24-P-300-0.65A

Features

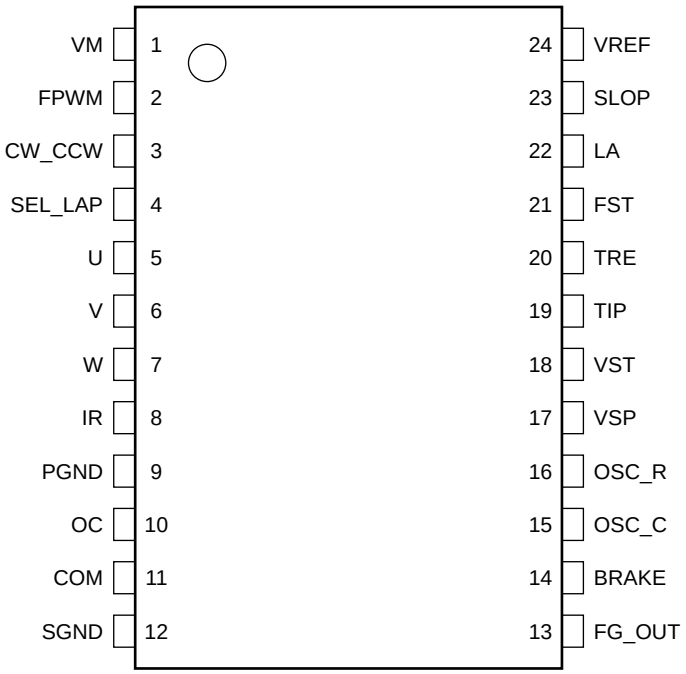
- Sensorless drive in three-phase full-wave mode
- PWM chopper control
- Controls the PWM duty cycle based on an analog input (7-bit ADC)
- Output current: I_{OUT} = 0.6 A typ. (1 A max)
- Power supply: VM = 4.5 V to 22 V (25 V max)
- Forward and reverse rotation
- Lead angle control (0°, 15° and 30°)
- Overlapping commutation (120°, 135° and 150°)
- Selectable duty cycle modulation period upon state transitions of phase signals
- Rotation speed detecting signal (FG_OUT)
- Adjustable startup settings
- Forced commutation frequency control ($f_{osc}/(6 \times 2^{17})$, $f_{osc}/(6 \times 2^{18})$ and $f_{osc}/(6 \times 2^{19})$)
- Selectable PWM frequency
- Restart feature
- Overcurrent protection (ISD)
- Thermal shutdown (TSD)
- Undervoltage lockout (LVD)
- Current limiter
- Short brake control

Note1: 8 pin (RS) of this product is sensitive to electrostatic discharge. When handling this product, protect the environment to avoid electrostatic discharge.

Note2: The following conditions apply to solderability:
About solderability, following conditions were confirmed
(1) Use of Sn-37Pb solder Bath
- solder bath temperature: 230°C
- dipping time: 5 seconds
- the number of times: once
- use of R-type flux

(2) Use of Sn-3.0Ag-0.5Cu solder Bath
- solder bath temperature: 245°C
- dipping time: 5 seconds
- the number of times: once
- use of R-type flux

Pin Assignment



Pin Description

Pin No.	Symbol	I/O	Description
1	VM	—	Motor power supply pin
2	FPWM	I	PWM frequency (f_{PWM}) select input (This pin has a pull-down resistor.) High : $f_{PWM} \simeq f_{osc}/128$ Example) $f_{PWM} \simeq 40$ kHz @ $f_{osc} = 5.1$ MHz Low, Open : $f_{PWM} \simeq f_{osc}/256$ Example) $f_{PWM} \simeq 20$ kHz @ $f_{osc} = 5.1$ MHz
3	CW_CCW	I	Rotation direction select input (This pin has a pull-down resistor.) High : Counterclockwise (U → W → V) Low, Open : Clockwise (U → V → W)
4	SEL_LAP	I	Overlapping commutation select pin (This pin has a pull-down resistor.) High : Overlapping commutation Low, Open : 120° commutation
5	U	O	U-phase output
6	V	O	V-phase output
7	W	O	W-phase output
8	IR	—	Connection pin for an output shunt resistor
9	PGND	—	Power ground pin
10	OC	I	Overcurrent detection input (This pin has a pull-down resistor.) All PWM output signals are stopped when OC ≥ 0.25 V (typ.).
11	COM	I	Connection pin for the center tap of the motor
12	SGND	—	Signal ground pin
13	FG_OUT	O	Rotation speed output pin (open-drain) This output is held low at startup and when an abnormality is detected. In sensorless mode, pulses are generated at 3 ppr according to the back-EMF. Note: 3 ppr = 3 pulses per electrical degree (With a four-pole motor, six pulses are generated per revolution.)
14	BRAKE	I	Short brake control pin (This pin has a pull-down resistor.) High : Short brake Low, Open : Normal operation
15	OSC_C	—	OSC_C: Connection pin for the oscillator capacitor OSC_R: Connection pin for the oscillator resistor Example: Internal oscillating frequency (f_{osc}) ≃ 5.1 MHz (typ.) when OSC_C = 68 pF and OSC_R = 20 KΩ.
16	OSC_R	—	
17	VSP	I	Motor speed control input (This pin has a pull-down resistor.) $0 \le VSP \le V_{AD}$ (L); 1 V (typ.) : 0% duty cycle V_{AD} (L) ≤ VSP ≤ V_{AD} (H); 4 V (typ.) : Sets the PWM duty cycle based on the analog input. V_{AD} (H) ≤ VSP ≤ VREF : 100% duty cycle (127/128)
18	VST	—	Duty cycle setting pin for DC excitation and forced commutation modes $0 \le VST \le V_{AD}$ (L); 1 V (typ.) : 0% duty cycle V_{AD} (L) ≤ VST ≤ V_{AD} (H); 4 V (typ.) : Sets the PWM duty cycle based on the analog input. V_{AD} (H) ≤ VST ≤ VREF : 100% duty cycle (127/128)
19	TIP	—	Connection pin for a capacitor to set the DC excitation time
20	TRE	—	Connection pin for a capacitor to set the restart time upon abnormality detection
21	FST	I	Forced commutation frequency select input (This pin has a pull-down resistor.) Forced commutation frequency (f_{ST}): cycles per second equivalent to an electrical degree FST = High = $f_{ST} \simeq f_{osc}/(6 \times 2^{17})$ Example) $f_{ST} \simeq 6.4$ Hz @ $f_{osc} = 5.1$ MHz FST = Middle = $f_{ST} \simeq f_{osc}/(6 \times 2^{18})$ Example) $f_{ST} \simeq 3.2$ Hz @ $f_{osc} = 5.1$ MHz FST = Low, Open = $f_{ST} \simeq f_{osc}/(6 \times 2^{19})$ Example) $f_{ST} \simeq 1.6$ Hz @ $f_{osc} = 5.1$ MHz
22	LA	I	Lead angle select input (This pin has a pull-down resistor.) LA = High ≃ 30° lead angle LA = Middle ≃ 15° lead angle LA = Low, Open ≃ 0° lead angle
23	SLOP	I	Modulation scheme select input for phase signal state transitions (This pin has a pull-down resistor.) SLOP = High ≃ modulation SLOP = Middle ≃ test mode SLOP = Low, Open ≃ No modulation
24	VREF	—	Reference voltage output; VREF = 5 V (typ.)

Functional Description

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Timing charts may be simplified for explanatory purposes.

1. Sensorless Drive Mode

Based on the analog voltage input at the VSP pin for a startup operation, the rotor is aligned to a known position in DC excitation mode. Then, the forced commutation signal is generated to start the motor rotation. As the motor rotates, the back-EMF occurs in each phase of the coil. When an input signal indicating the polarity of three phase voltage of the motor, including the back-EMF, is detected as a position signal, the motor driving signal is automatically switched from forced commutation signal to the normal commutation PWM signal that is based on the position signal input (back-EMF). Then, a BLDC motor starts running in sensorless commutation mode.

2. Startup Operation

At startup, no induced voltage is generated due to the stationary motor, and the rotor position cannot bedetected in sensorless mode. Therefore, the TB6633FNG rotor is first aligned to a known position in DC excitation mode for an appropriate period of time, and then the motor is started in forced commutation mode.

The DC excitation time is determined via the TIP pin. The forced commutation frequency is determined via the FST pin. The duty cycles for DC excitation and forced commutation modes are determined by the VST voltage. For sensorless mode, the PWM duty cycle is determined by the VSP value. A speed-control voltage should be applied to the VSP pin to start and stop the motor operation, and to control the motor speed. Since the time settings and startup torques (output duty cycle) for DC excitation and forced commutation vary depending on the motor type and load, they should be adjusted experimentally.

1) DC Excitation Mode

The DC excitation time is determined via the TIP pin.

DC excitation time: $T_2 = C_2 \times$ TIP pin voltage/TIP pin charge current

$C_2 = 0.1\ \mu F$, $T_2 = 0.1\ \mu F \times 3$ V (typ.)/3 μA (typ.) = 0.1 s

2) Forced Commutation Mode

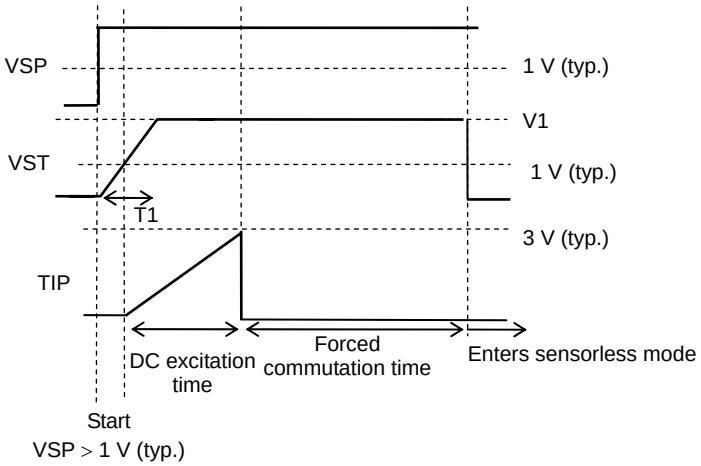
The forced commutation frequency is determined via the FST pin.

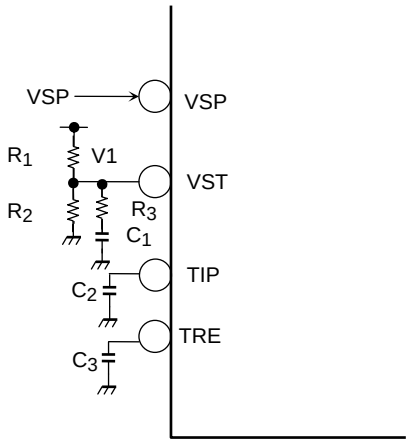
(The FST pin has a pull-down resistor.)

FST = High = Forced commutation frequency $f_{ST} \simeq f_{osc}/(6 \times 2^{17})$

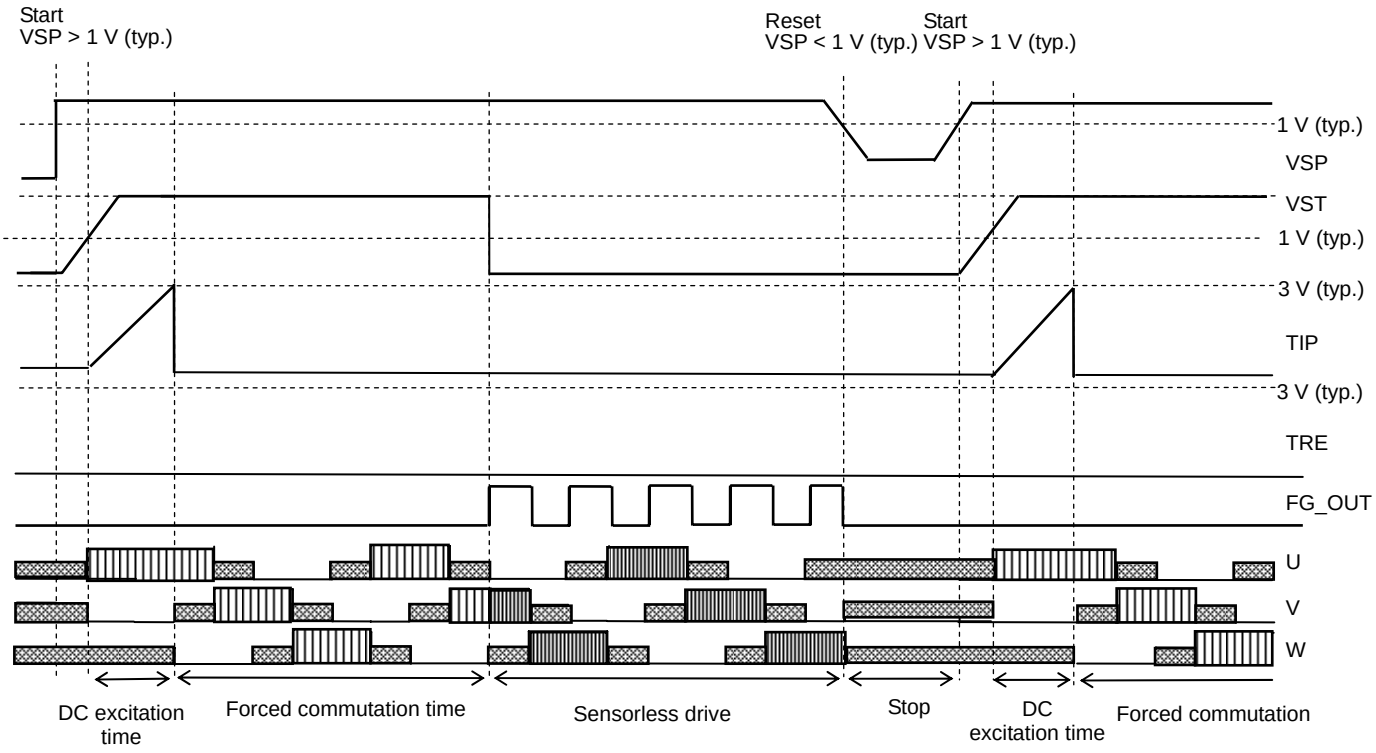
FST = Middle = Forced commutation frequency $f_{ST} \simeq f_{osc}/(6 \times 2^{18})$

FST = Low, Open = Forced commutation frequency $f_{ST} \simeq f_{osc}/(6 \times 2^{19})$





3) Timing Diagram of the Startup Operation (CW_CCW = Low: Clockwise rotation)



Output duty cycle determined by the VSP voltage

Output duty cycle determined by the VST voltage

OFF (High impedance)

3. Restart Operation

When any abnormality is detected, output signals are turned off (high impedance) during the operation restart time.

The following events are detected as abnormalities:

1. The forced commutation time exceeds eight electrical-degree period.
2. The ISD circuit is activated.
3. The TSD circuit is activated.
4. The rotation speed falls below the forced commutation frequency for sensorless mode.
5. The short brake mode is exited.
6. The input is switched at CW_CCW pin for sensorless mode.
7. Maximum commutation frequency (FMAX)

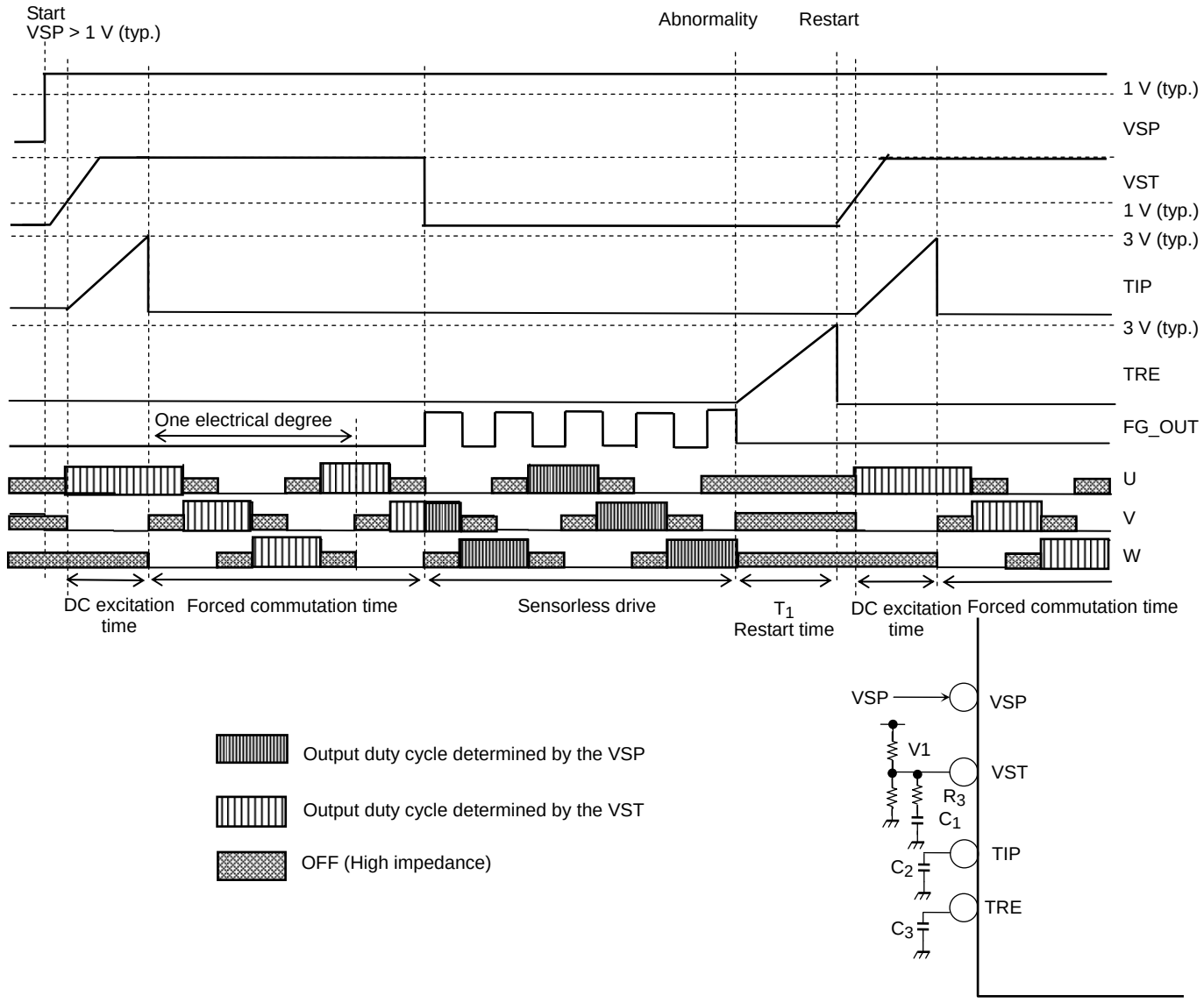
FST=High=FMAX=$f_{osc}/(6 \times 2^{11})$ Example) FMAX=400Hz per electrical degree @ f_{osc} = 5.1 MHz
FST=Middle=FMAX=$f_{osc}/(6 \times 2^{11})$ Example) FMAX=400Hz per electrical degree @ f_{osc} = 5.1 MHz
FST=Low=FMAX=$f_{osc}/(6 \times 2^{12})$ Example) FMAX=200Hz per electrical degree @ f_{osc} = 5.1 MHz

The restart time is determined via the TRE pin as follows:

Restart time: $T_1 = C_3 \times$ TRE pin voltage/TRE pin charge current
C_3 = 0.1 μF, T_1 = 0.1 μF × 3 V (typ.)/3 μA (typ.) = 0.1 s (typ.)

For example, when the motor does not rotate due to motor locking or when a mode transition from forced commutation mode to sensorless mode does not properly occur, the TB6633FNG begins cycling into the following operation:

Operation start when VSP >1 V (typ.) → DC excitation time → Forced commutation time of eight electrical-degree period → Restart time → DC excitation time …



4. PWM Frequency

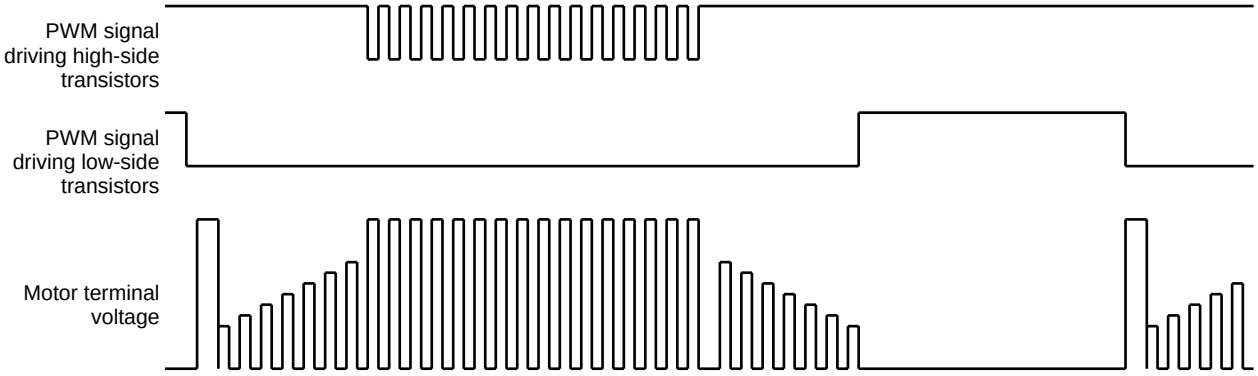
The PWM frequency is determined by the logic level of the FPWM pin (which has a pull-down resistor).

FPWM: High : $f_{PWM} = f_{osc}/128$

FPWM: Low, Open : $f_{PWM} = f_{osc}/256$

The PWM frequency must be sufficiently high relative to the electrical frequency of the motor and within the range permitted by the switching characteristics of the driver circuit.

The PWM signal switches on and off the high-side transistors.



5. Motor Speed Control Pins (VSP and VST)

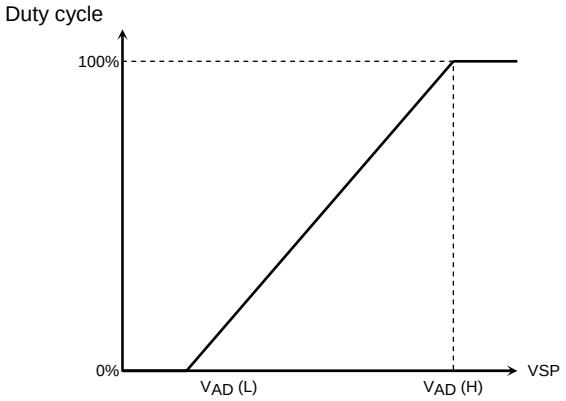
The startup sequence is executed when the VSP voltage reaches 1 V (typ.); while the motor operation is reset when the VSP voltage falls below 1 V (typ.).

Analog voltages applied to the VSP and VST pins are converted by a 7-bit AD converter and used to control the duty cycle of the PWM.

$0 \leq$ (VSP, VST) $\leq$ VAD (L) $\rightarrow$ Duty = 0%

V_{AD} (L) $\leq$ (VSP, VST) $\leq V_{AD}$ (H) $\rightarrow$ Figure on the under (1/128 to 127/128)

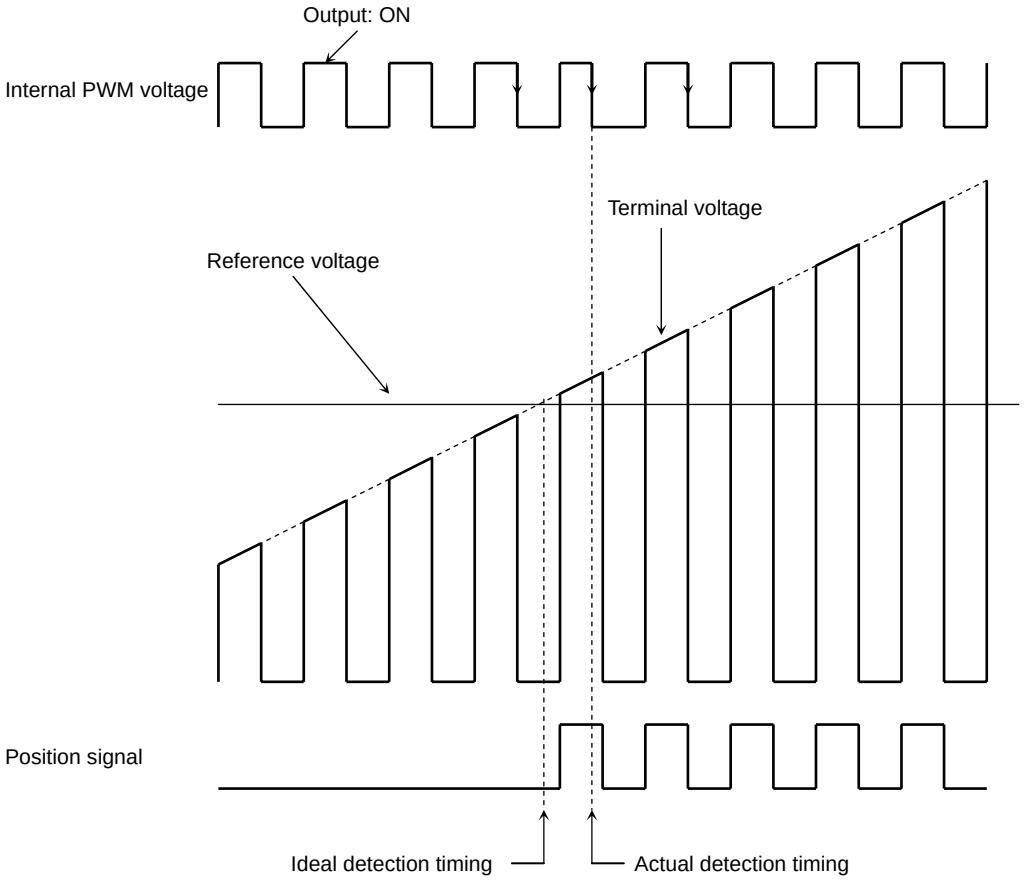
V_{AD} (H) $\leq$ (VSP, VST) $\leq$ VREF $\rightarrow$ Duty = 100% (127/128)



6. Motor Position Detection Error

The position detection is performed synchronizing with the PWM signal generated in the IC. Thus, a position detection error related to the PWM signal frequency is induced. Care should be taken when the TB6633FNG is used in high-speed motor application.
The detection is performed on the falling edge of the PWM signal. An error is recognized when the terminal voltage exceeds the reference voltage.

Detection lag < $1/f_p$ f_p: PWM frequency = $f_{osc}/256$, $f_{osc}/128$ f_{osc}: Internal oscillating frequency



7. Commutation Control

In forced commutation mode at startup, the TB6633FNG is configured for 120° commutation with a lead angle of 0°, and with no duty cycle modulation upon state transitions of phase signals. Then, when the motor operation enters sensorless mode, its commutation waveform automatically changes to the one specified by the LA, SEL_LAP and SLOP pins.

The relationships between the logic level of the LA pin and the commutation lead angle are as follows:

LA = High: 30° lead angle

LA = Middle: 15° lead angle

LA = Low: 0° lead angle

When SEL_LAP = Low, the TB6633FNG runs in 120° commutation mode; when SEL_LAP = High, it runs in overlapping commutation mode.

In overlapping commutation mode, there occurs an overlapping period due to the lengthened commutation time between the zero cross point and the 120° commutation timing upon state transitions of phase signals. This period varies depending on the lead angle setting.

At the same time, the logic level of the SLOP pin specifies the number of steps that are taken for changing the PWM duty cycle as determined by the VSP pin upon state transitions of phase signals.

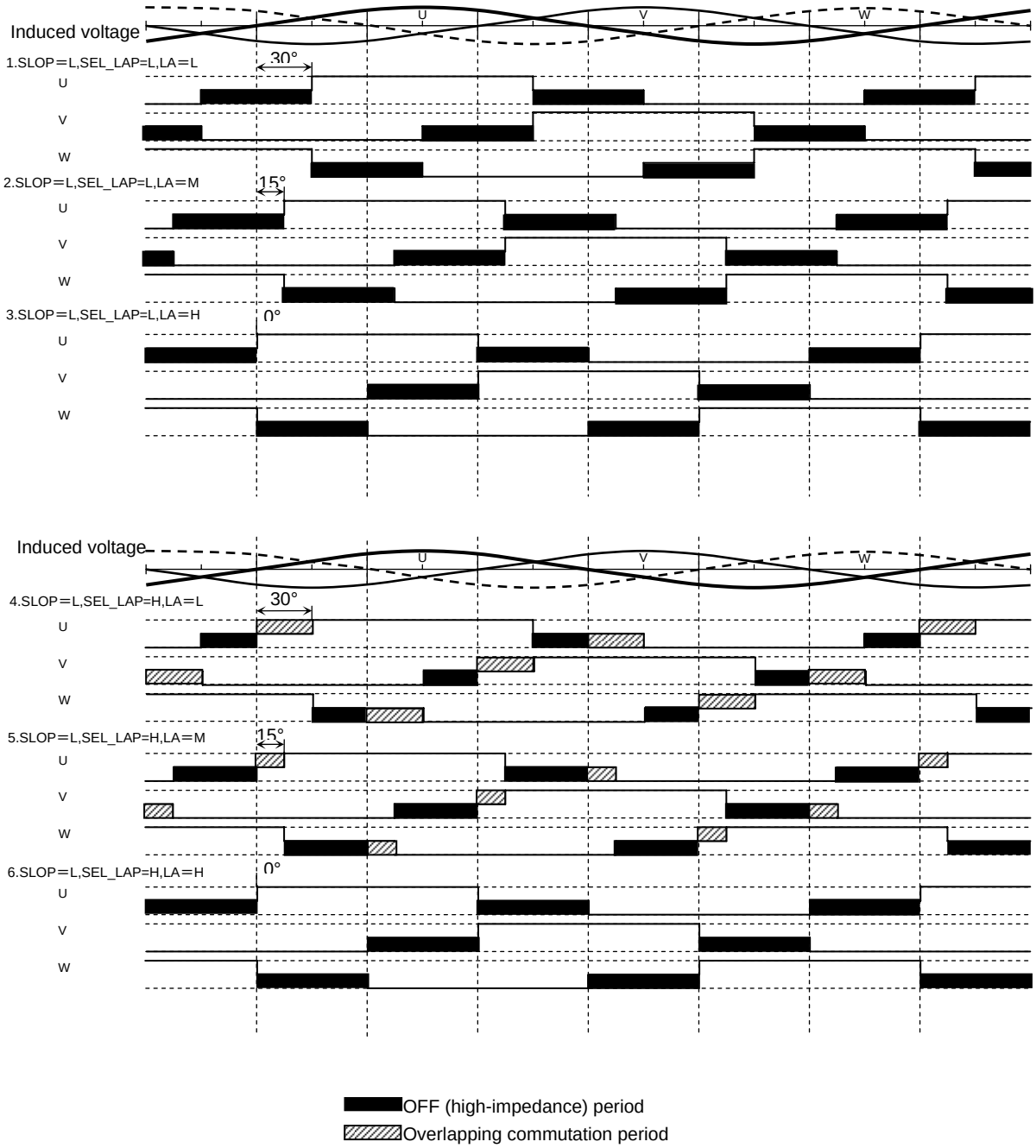
SLOP = High: Duty cycle change upon state transitions of phase signals.

SLOP = Middle:Test mode

SLOP = Low: Duty cycle does not change upon state transitions of phase signals.

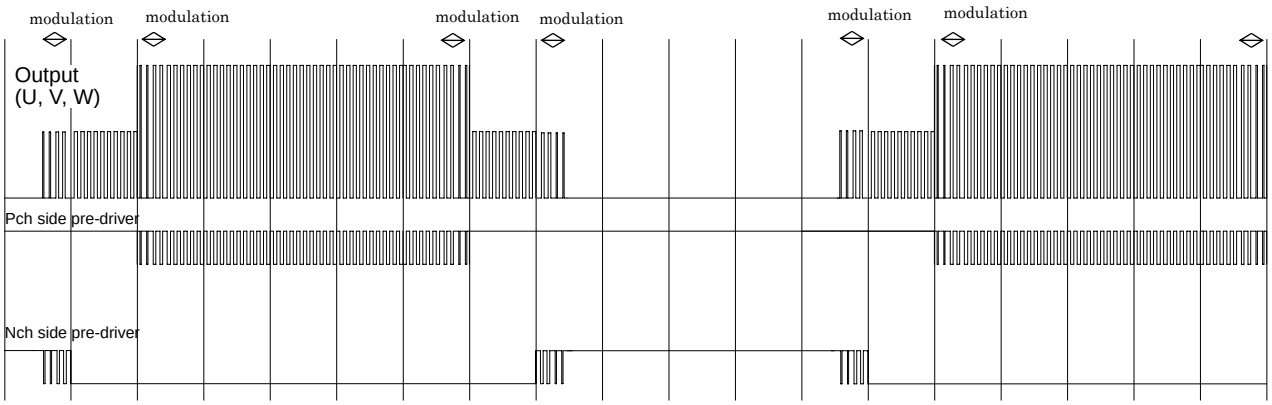
SLOP Pin	SEL_LAP Pin	LA Pin	Modulation period for phase signal state transitions	Commutation Angle	Lead Angle	Timing Waveform No.
H	H	H	No modulation	120°	30°	6
		M		135°	15°	5
		L	Modulation	150°	0°	7
	L	H	No modulation	120°	30°	3
		M			15°	2
		L			0°	1
M	Test mode					
L	H	H	No modulation	120°	30°	6
		M		135°	15°	5
		L		150°	0°	4
	L	H		120°	30°	3
		M			15°	2
		L			0°	1

1) Timing diagrams of commutation waveforms (CW_CCW = Low: Clockwise rotation)

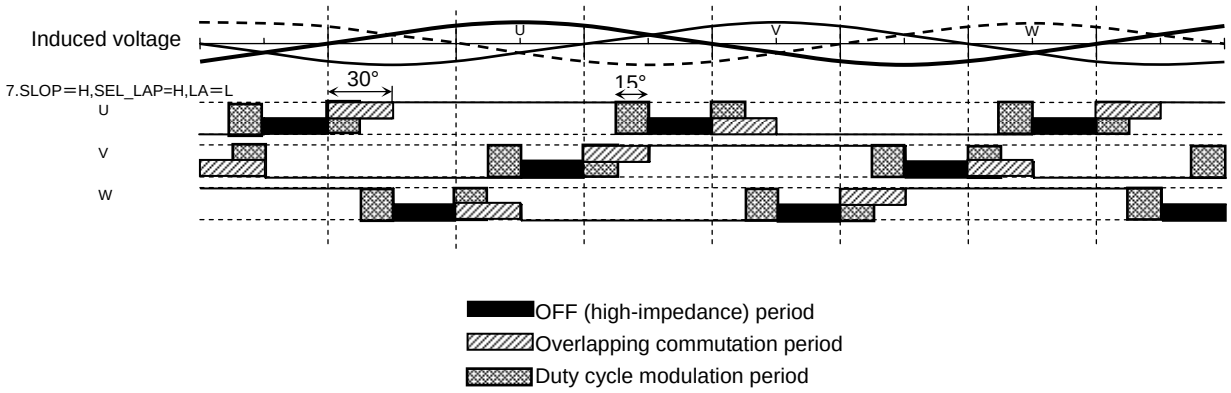


2) Modulated waveforms upon state transitions of phase signals

Modulation upon phase signal state transitions (150° commutation)SLOP=H,SEL_LAP=H,LA=L)



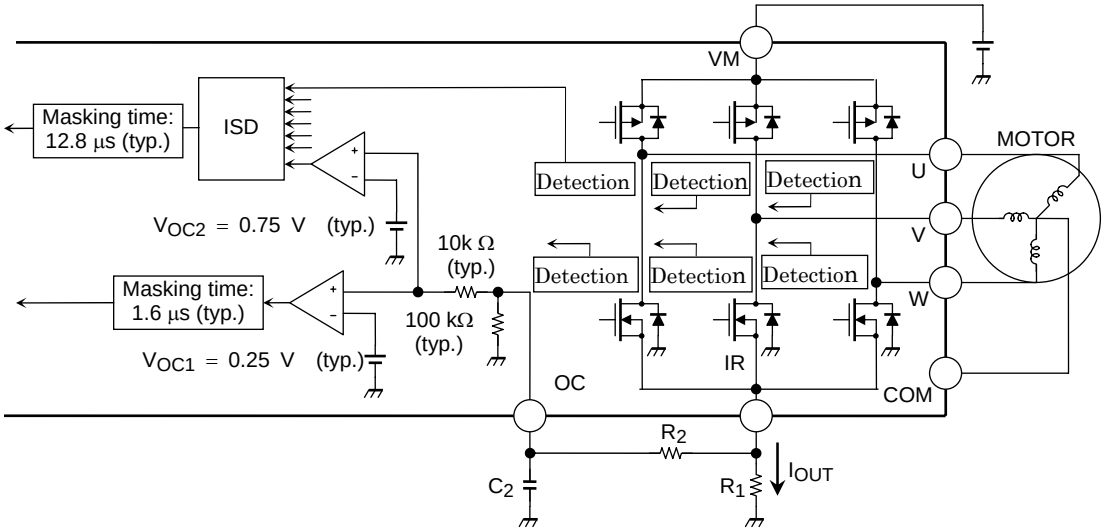
Timing diagrams of commutation waveforms (CW_CCW = Low: Clockwise rotation)



8. Current Limiter

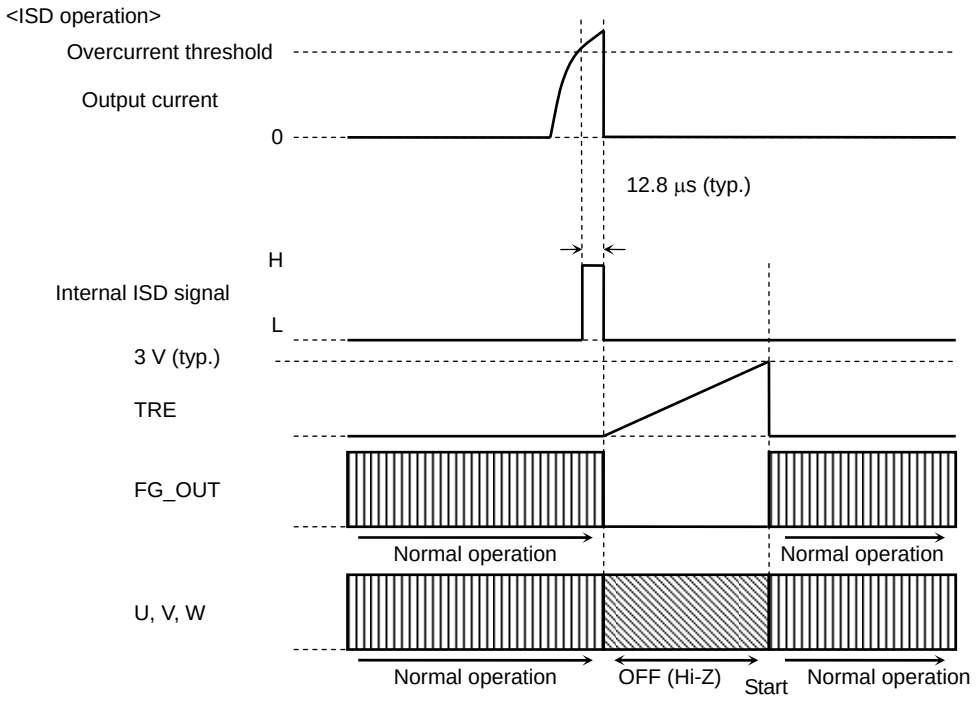
The current limiter circuit limits the current by turning the high-side transistors off. These transistors are turned back on again when the PWM signal is turned on.
The output current is monitored as a voltage across R_1. If it exceeds the rated V_{OC1} voltage (0.25 V typ.), the current limiter is activated.
The current value that trips the overcurrent protection circuit is calculated as:
I_{OUT} = Overcurrent detection voltage V_{OC}/Resistor value R_1
Though a masking time of 1.6 μs (typ.) is provided, R_2 and C_2 used as an RC filter should be adjusted properly to prevent the malfunction of the current limiter circuit due to the PWM switching noise.

Example) When R_1 = 0.3 Ω, I_{OUT} (typ.) = 0.25 V (typ.)/0.3 Ω ≃ 0.83 A



9. Overcurrent Protection (ISD) Circuit

The TB6588FG incorporates the overcurrent protection circuit that monitors the current flowing through six output power transistors.
If a current of between 1.0 A and 3.0.A is sensed for 12.8 μs (typ.) or longer at any one of six transistors, all output transistors are turned off (Hi-Z).
They are re-enabled after the restart time that is determined by the TRE pin has elapsed.
And if it exceeds the rated V_{OC2} voltage (0.75V typ.), all output transistors are turned off (Hi-Z).

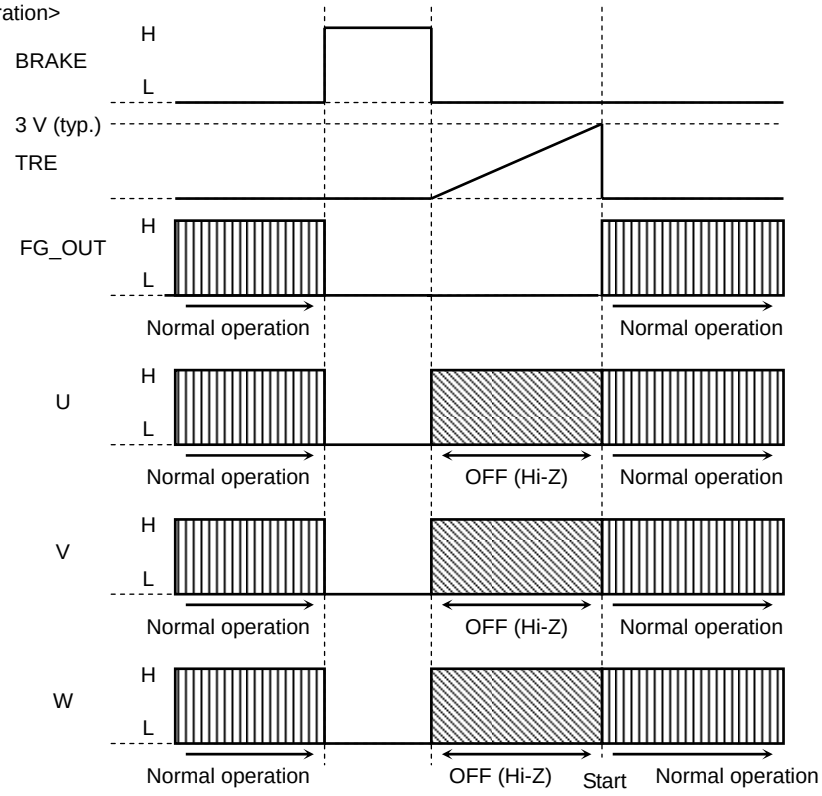


Note: The ISD circuit is activated if the absolute maximum current rating is violated. Note that the circuit is provided as an auxiliary only and does not necessarily provide the IC with a perfect protection from damages due to overcurrent caused by power fault, ground fault, load-short and the like.

10. Short Brake Operation

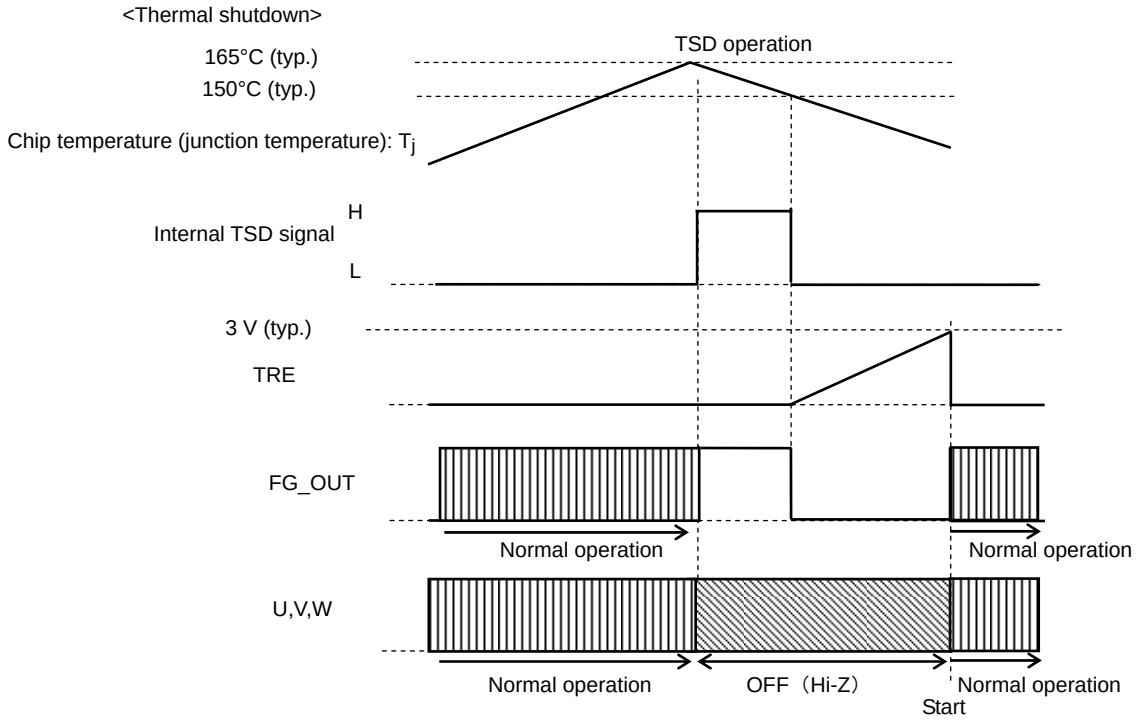
Setting the BRAKE pin High drives all the outputs (U, V and W) Low and the TB6633FNG enters short brake mode. This allows the motor to be quickly stopped. The outputs are re-enabled when the restart time that is specified by the TRE pin has elapsed after the High-to-Low transition of the BRAKE.

<Short brake operation>



11. Thermal Shutdown (TSD) Circuit

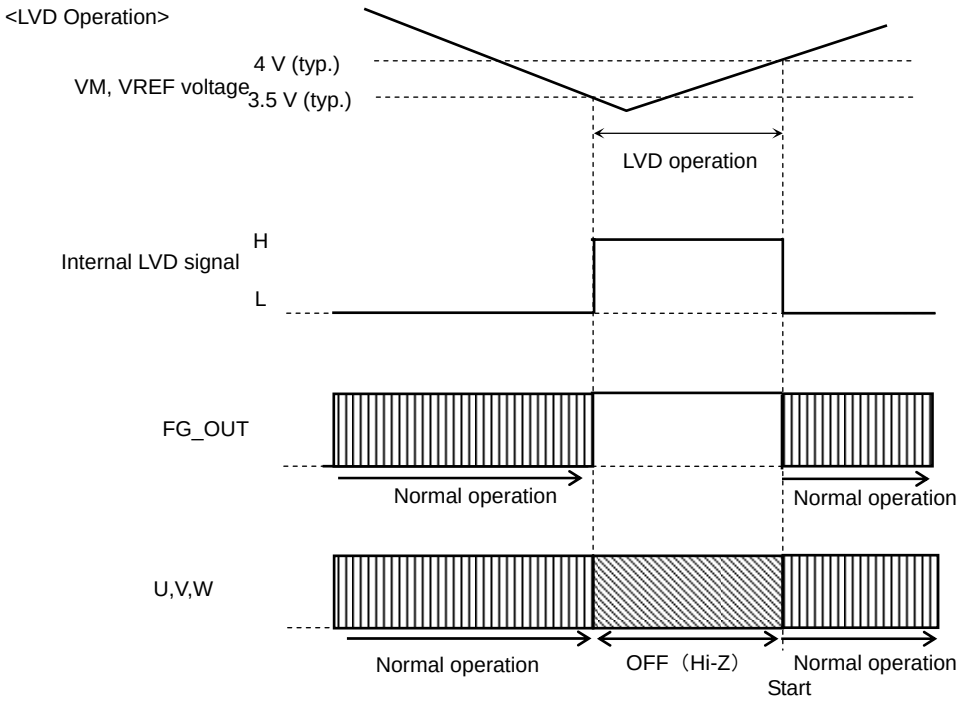
The TB6633FNG incorporates a thermal shutdown circuit. When the junction temperature (T_j) exceeds 165°C (typ.), the output transistors are turned off (Hi-Z). The output transistors are turned on after the restart time that is specified by the TRE pin has elapsed.
The IC has 15°C of temperature hysteresis.



Note: The TSD circuit is activated if the absolute maximum junction temperature rating (T_j) of 150°C is violated. Note that the circuit is provided as an auxiliary only and does not necessarily provide the IC with a perfect protection from any kind of damages.

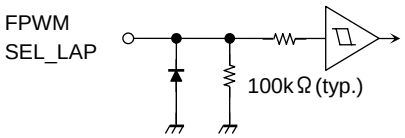
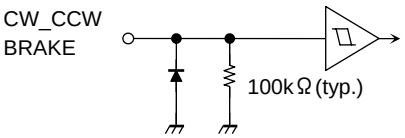
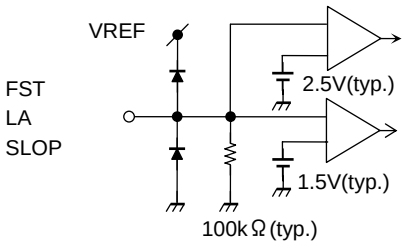
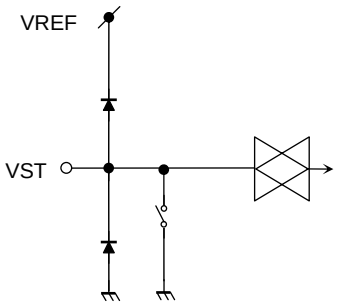
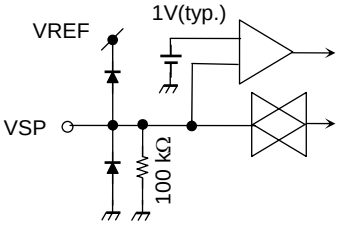
12. Undervoltage Lockout Circuit

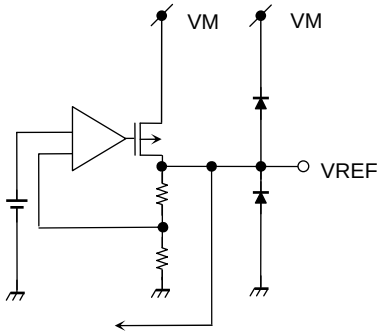
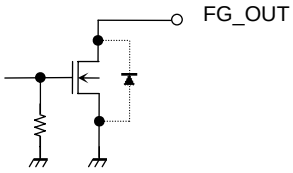
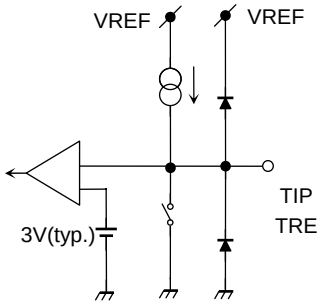
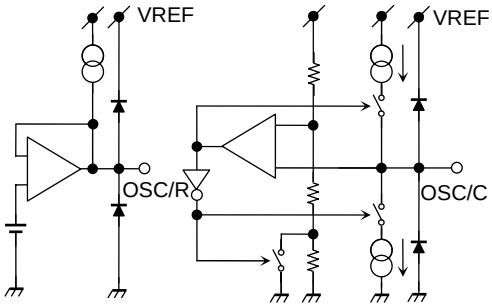
The TB6633FNG includes an undervoltage lockout circuit, which turns the control logic off to put the output transistors in the high-impedance state when VM or VREF decreases to 3.5 V (typ.) or lower.
The output transistors are automatically turned on when VM or VREF increases past the lockout threshold, which is raised to 4 V by a hysteresis of 0.5 V.

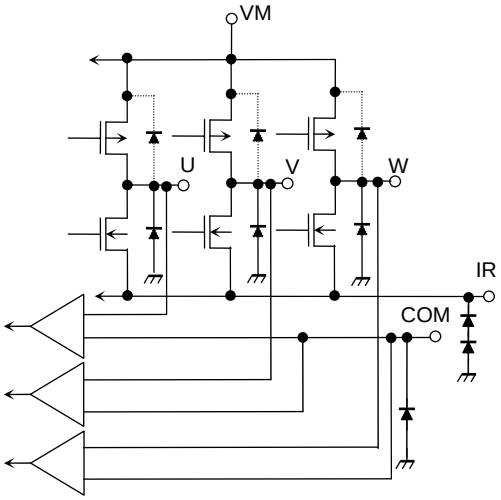
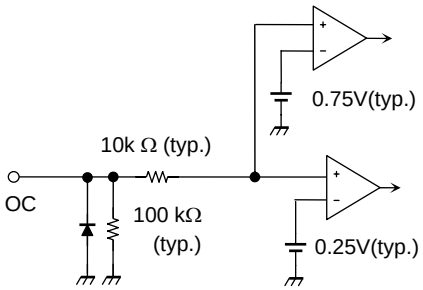


I/O Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Pin No.	I/O Signal	I/O Internal Circuit
FPWM(2) SEL_LAP(4)	Input H: 2 V (min) L: 0.8 V (max)	
CW_CCW(3) BRAKE(14)	Input H: 2 V (min) L: 0.8 V (max)	
FST (21) LA(22) SLOP(23)	Input H: 4 V (min) M:2V (min) 3V (max) L: 0.8 V (max)	
VST(18)	Duty cycle setting pin for DC excitation and forced commutation modes $0 \le VST \le V_{AD}$ (L); 1 V (typ.) 0% duty cycle V_{AD} (L) ≤ VST ≤ V_{AD} (H); 4 V (typ.) Sets the PWM duty cycle based on the analog voltage input. V_{AD} (H) ≤ VST ≤ VREF 100% duty cycle (127/128)	
VSP(17)	Motor speed control input $0 \le VSP \le V_{AD}$ (L); 1 V (typ.) 0% duty cycle V_{AD} (L) ≤ VSP ≤ V_{AD} (H); 4 V (typ.) Sets the PWM duty cycle based on the analog voltage input. V_{AD} (H) ≤ VSP ≤ VREF 100% duty cycle (127/128)	

Pin No.	I/O Signal	I/O Internal Circuit
VREF(24)	Reference voltage output VREF = 5 V (typ.)	
FG_OUT(13)	Rotation speed output pin Open-drain output An externally attached pull-up resistor enalbes the High output.	
TIP(19) TRE(20)	TIP:Connection pin for a capacitor to set the DC excitation time TRE:Connection pin for a capacitor to set the restart time upon abnormality detection C = 0.1μF, 0.1 μF × 3 V (typ.)/3 μA (typ.) = 0.1 s (typ.)	
OSC/C(15) OSC/R(16)	Connection pin for the oscillator (f_{osc}) ≃ 5.1 MHz (typ.) when OSC_C = 68 pF and OSC_R = 20 KΩ.	

Pin No.	I/O Signal	I/O Internal Circuit
VM(1) U (5) V(6) W(7) IR(8) COM(11)	U,V,W-phase output VM:Motor power supply pin COM:Connection pin for the center tap of the motor IR:Connection pin for an output shunt resistor	
OC(10)	Overcurrent detection input All PWM output signals are stopped when OC ≥ 0.25 V (typ.).	

Absolute Maximum Ratings (Note) (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	VM	25	V
Input voltage	V_{IN1} (Note 1)	−0.3 to 6.0	V
	V_{IN2} (Note 2)	−0.3 to 25	V
Output voltage	V_{OUT1} (Note 3)	25	V
	V_{OUT2} (Note 4)	6.0	V
Output current	I_{OUT1} (Note 5)	1 (Note 8)	A
	I_{OUT2} (Note 6)	5	mA
	I_{OUT3} (Note 7)	5	mA
Power dissipation	P_D	0.78 (Note 9)	W
Operating temperature	T_{opr}	−40 to 85	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
Please use the TB6633FNG within the specified operating ranges.

Note 1: V_{IN1} is applicable to the voltage at the following pins: FPWM, VSP, CW_CCW, LA, OC, SEL_LAP, FST, BRAKE and SLOP

Note 2: V_{IN2} is applicable to the voltage at the COM pin.

Note 3: V_{OUT1} is applicable to the voltage at the following pins: U, V and W

Note 4: V_{OUT2} is applicable to the voltage at the FG_OUT pin.

Note 5: I_{OUT1} is applicable to the current at the following pins: U, V and W

Note 6: I_{OUT2} is applicable to the current at the FG_OUT pin.

Note 7: I_{OUT3} is applicable to the current at the VREF pin.

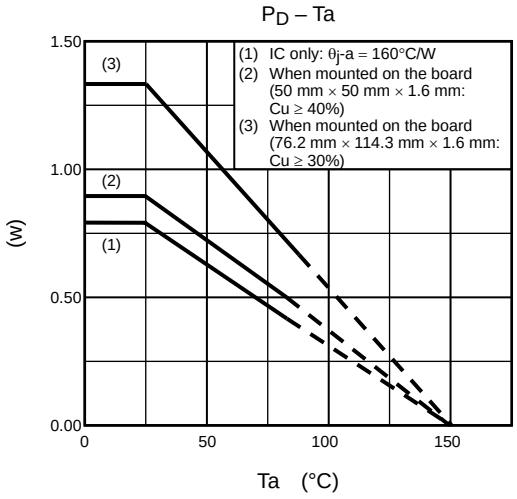
Note 8: Output current may be limited by the ambient temperature or the device implementation.
The maximum junction temperature should not exceed T_{jmax} = 150°C

Note 9: Measured for the IC only. (Ta = 25°C)

Operating Ranges

Characteristics	Symbol	Min	Typ.	Max	Unit
Power supply voltage 1	VM_{opr1}	5.5	12	22	V
Power supply voltage 2	VM_{opr2}	4.5	5	5.5	V

Package Power Dissipation



Electrical Characteristics
(Ta =25°C, VM = 12 V, unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Static power supply current at VM	I_M	VSP = VST=0V, IR=TIP =COM=GND, The OSC_C = 68 pF, OSC_R = 20kΩ	—	3.5	6	mA
Dynamic power supply current at VM	$I_{M\ (opr)}$	VSP =VST= 2.5 V, IR=TIP =COM=GND, The OSC_C = 68 pF, OSC_R = 20kΩ	—	4	7	mA
Input current	I_{IN1} (H)	V_{IN} = 5 V FPWM, CW_CCW, SEL_LAP, BRAKE, FST, SLOP, LA	—	50	75	μA
	I_{IN1} (L)	V_{IN} = 0 V, FPWM, CW_CCW, SEL_LAP, BRAKE, FST, SLOP, LA	−1	0	—	
	I_{IN2} (H)	V_{IN} = 5 V, VSP	—	50	75	
	I_{IN2} (L)	V_{IN} = 0 V, VSP	−1	0	—	
Input voltage	V_{IN1} (H)	FPWM, CW_CCW, SEL_LAP, BRAKE	2.0	—	5.5	V
	V_{IN1} (L)		GND	—	0.8	
	V_{IN2} (H)	FST, SLOP, LA	4	—	VREF+ 0.3	
	V_{IN2} (M)		2	—	3	
	V_{IN2} (L)		GND	—	1	
Input voltage hysteresis	Vhys	FPWM, CW_CCW, SEL_LAP, BRAKE	—	0.45	—	V
Charge current at the TIP and TRE pins	Ich	OSC_R = 20 kΩ	2.4	3	3.6	μA
Capacitor charge time at the TIP and TRE pins	Tipre	TIP = 1 μF, TRE=1 μF, OSC_R = 20 kΩ	—	1	—	s
Detection voltage at the TIP and TRE pins	V_{DET}	—	2.8	3	3.2	V
COM input current	I_{COM}	COM=6V,VSP=VST=2.5V	−1	0	1	μA
Low-level FG_OUT output voltage	V_{FG_OUT}	I_{FG_OUT} = 5 mA	GND	—	0.5	V
FG_OUT leakage current	I_{LFG_OUT}	V_{FG_OUT} = 5.5 V	—	0	10	μA
Output ON-resistance at the U, V and W pins	R_{ON1} (H)	I_{OUT} = 0.6 A	—	0.4	0.65	Ω
	R_{ON1} (L)	I_{OUT} = −0.6 A	—	0.4	0.65	

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
	R_{ON2} (H)	I_{OUT} = 1.0 A	—	0.4	0.65	
	R_{ON2} (L)	I_{OUT} = −1.0 A	—	0.4	0.65	
	R_{ON3} (H)	I_{OUT} = 0.6 A VM=4.5V	—	0.45	0.75	
	R_{ON3} (L)	I_{OUT} = −0.6 A VM=4.5V	—	0.45	0.75	
	R_{ON4} (H)	I_{OUT} = 1.0 A VM=4.5V	—	0.45	0.75	
	R_{ON4} (L)	I_{OUT} = −1.0 A VM=4.5V	—	0.45	0.75	
Output leakage current at the U, V and W pins	I_L (H)	V_{OUT} = 0 V	—	0	10	μA
	I_L (L)	V_{OUT} = 25 V	—	0	10	
Output diodes' forward voltage at the U, V and W pins	V_F (H)	I_{OUT} = 1.0 A	—	1.0	1.4	V
	V_F (L)	I_{OUT} = −1.0 A	—	1.0	1.4	
VSP reset input voltage	V_{VSPR}	—	0.9	1.0	1.1	V
PWM input voltage	V_{AD} (L)	VSP=VST, FPWM = L OSC_C =68pF, OSC_R = 20 kΩ	0.9	1.0	1.1	V
	V_{AD} (H)		3.6	4.0	4.2	
OC pin voltage for current detection	V_{OC1}	—	0.225	0.25	0.275	V
OC pin voltage threshold for overcurrent detection	V_{OC2}	—	0.675	0.75	0.825	V
PWM frequency	F_{C1} (H)	FPWM = H OSC_C = 68 pF, OSC_R = 20 kΩ	36	40	44	kHz
	F_{C1} (L)	FPWM = L OSC_C = 68 pF, OSC_R = 20 kΩ	18	20	22	
OSC frequency	OSC	OSC_C = 68 pF, OSC_R = 20 kΩ	4.55	5.1	5.65	MHz
ISD trip threshold	I_{ISD}	—	—	2	—	A
Thermal shutdown	TSD	—	—	165	—	°C
	TSDhys	Thermal shutdown hysteresis	—	15	—	
UVLO trip threshold voltage at the VM pin	VM_{LVD}	—	—	3.5	—	V
UVLO recovery voltage at the VM pin	VM_{LVDR}	—	—	4.0	—	V
UVLO trip threshold voltage at the VREF pin	V_{RELVD}	—	—	3.5	—	V
UVLO recovery voltage at the VREF pin	V_{RERLVD}	—	—	4.0	—	V
VREF output voltage1	VREF1	IVREF = −5 mA	4.5	5	5.5	V
VREF output voltage2	VREF2	IVREF = −5 mA VM=4.5V	4.0	4.3	4.5	V

Application Circuit Example

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

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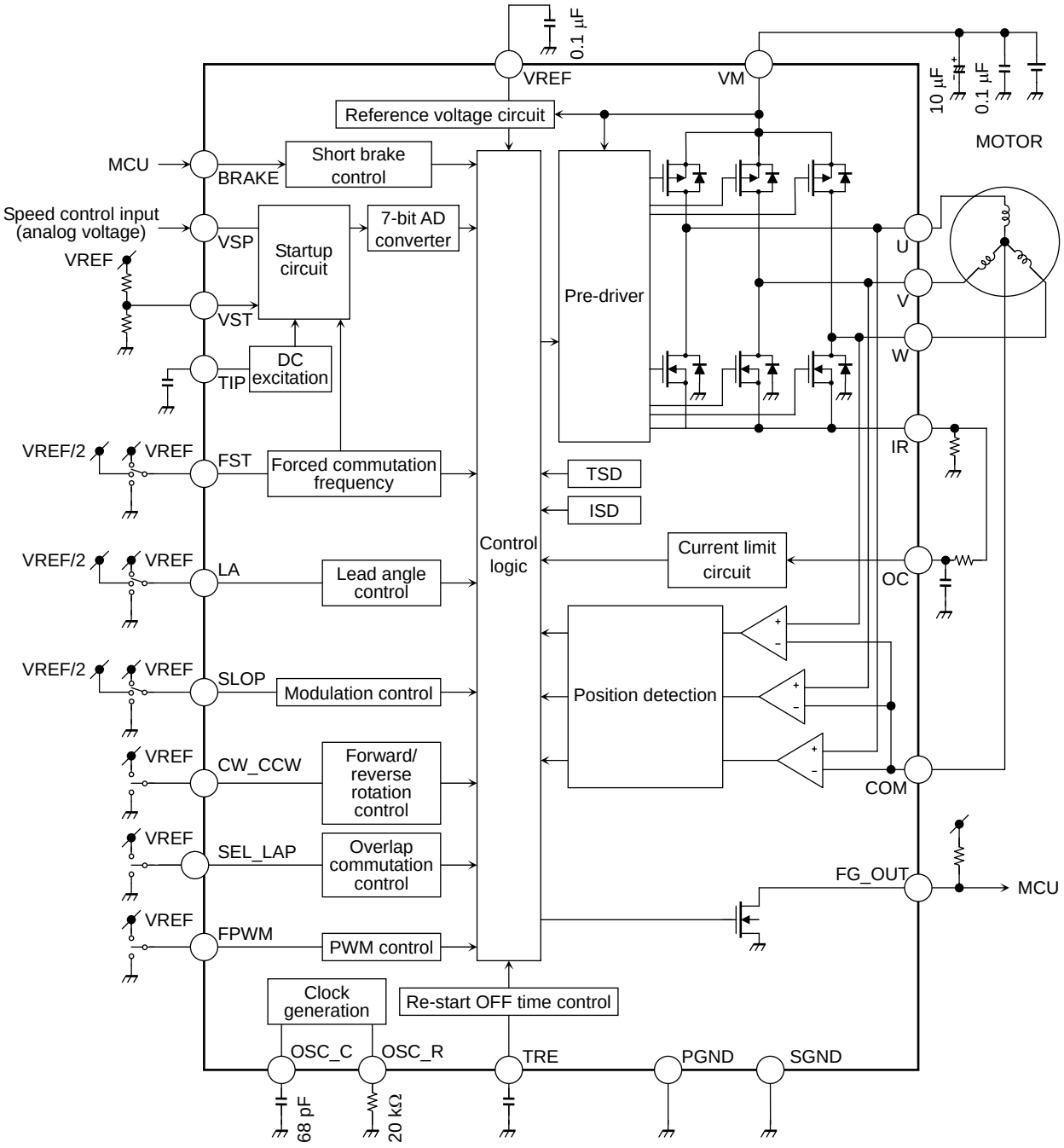
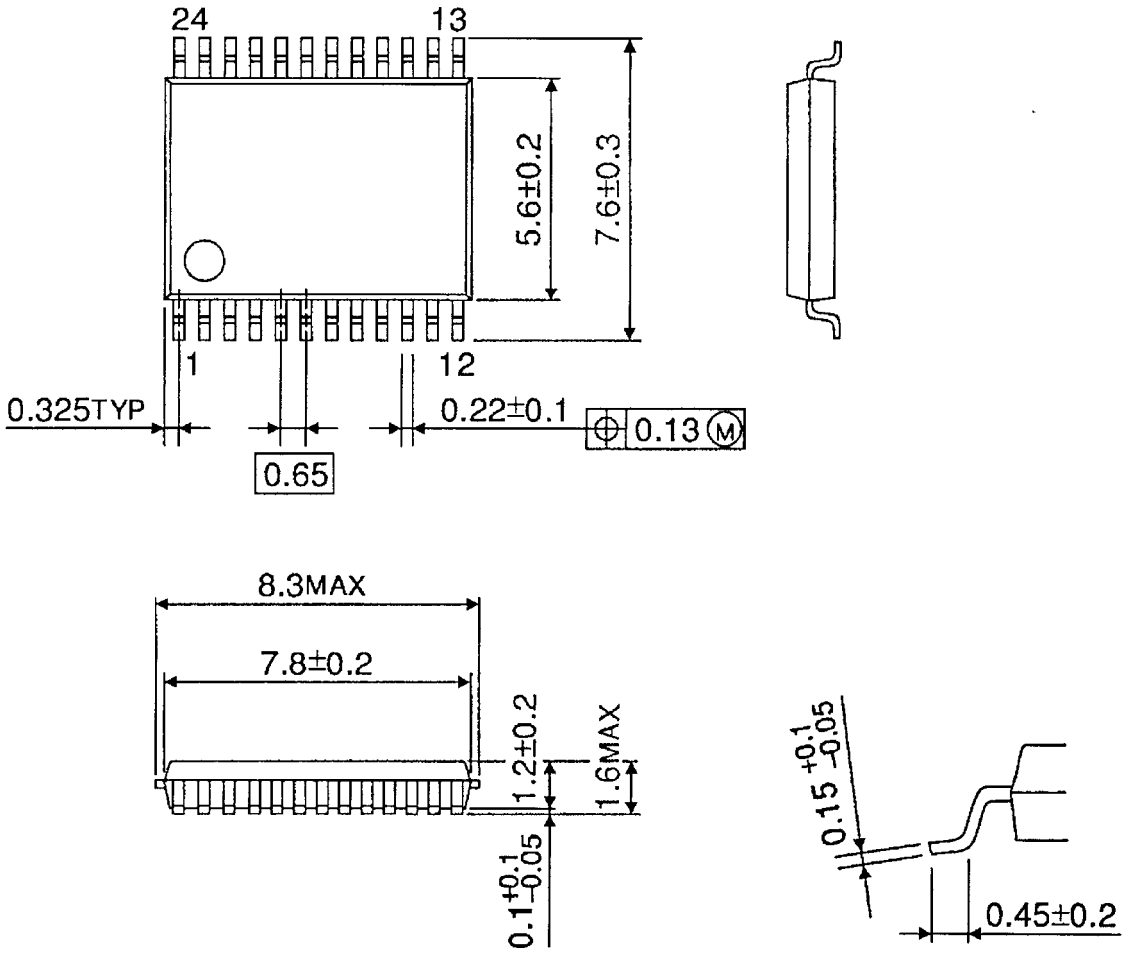


Package Dimensions

SSOP24-P-300-0.65A Unit : mm



Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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