Terawins, Inc.

Engineering Change Notice
Version 1.01

June 1, 2009

T107BL
Engineering Change Notice

Contents

1 New Features and Changes

The following sections describe the new features and bugs that have been fixed

1.1 T107DL and T107BL pin out diagram

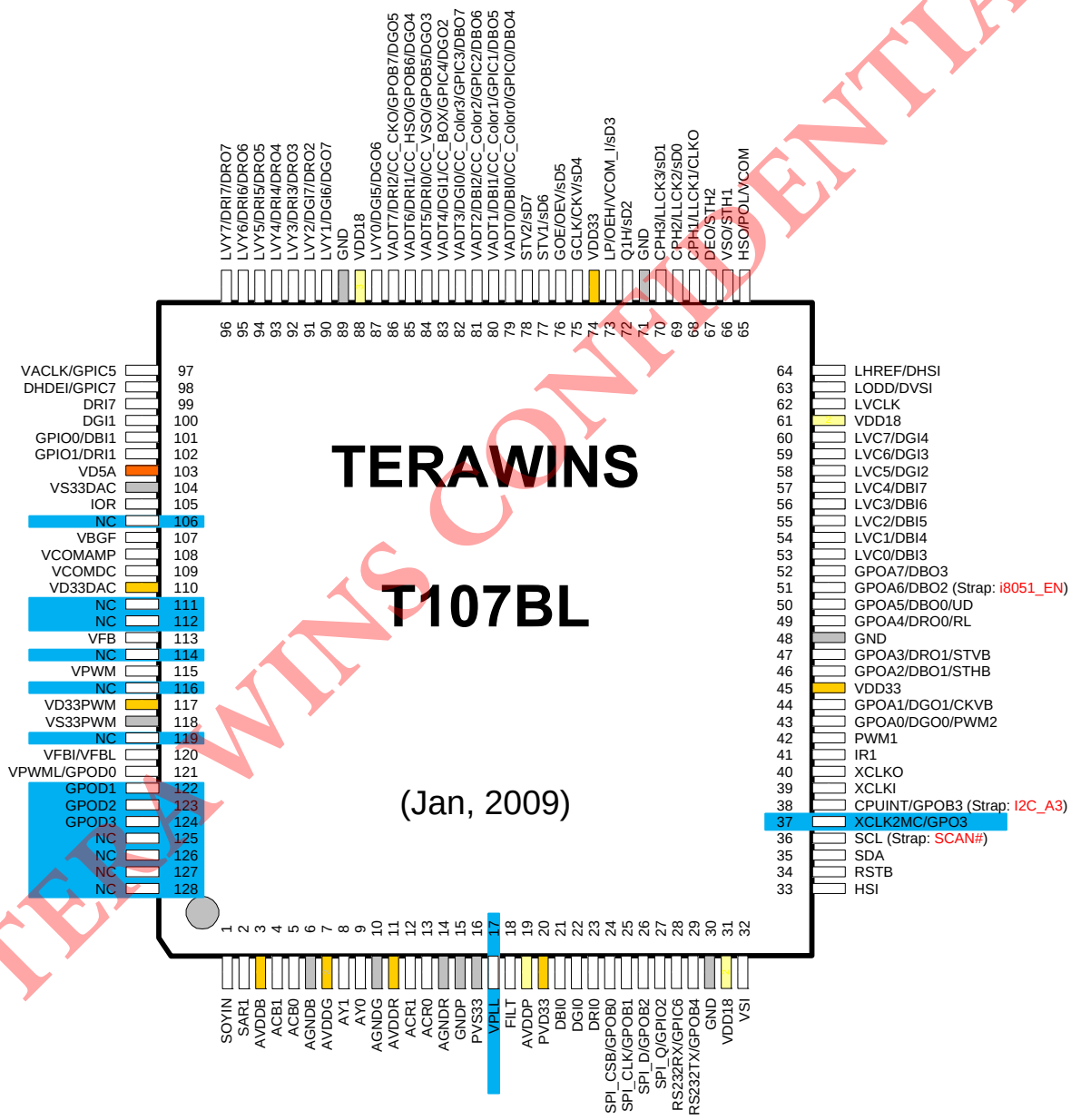

Figure 1-1 T107BL pinout diagram

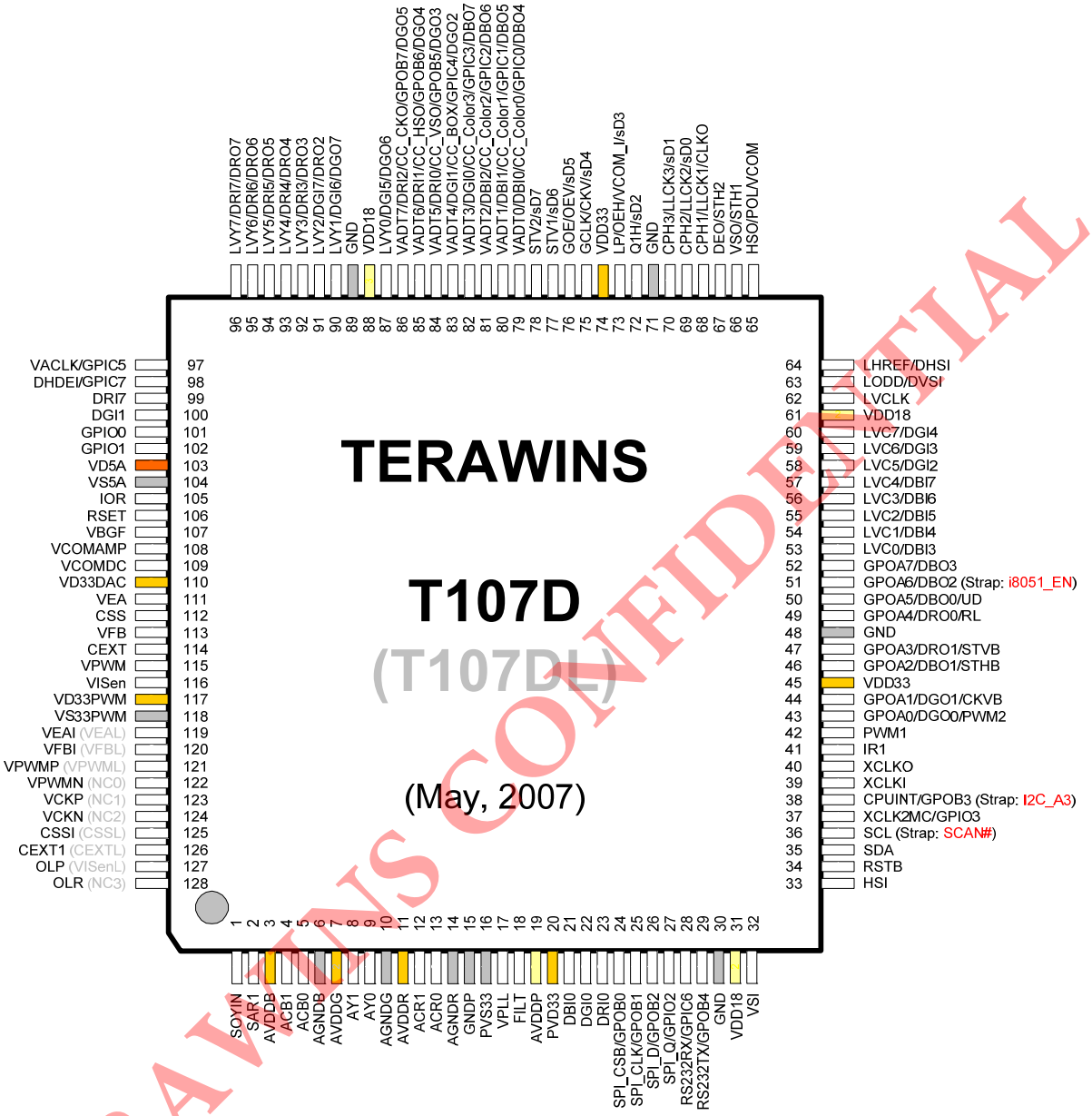

Figure 1-2 T107DL pinout diagram.

1.1.1 GPIO3 changed to GPO3

GPIO3 of T107L was changed to GPO3 in T107BL in which remove the GPI function.

1.2 Application circuit differences

1.2.1 LPLL power supply circuit

T107DL's AVDDP is powered by VDD 1.8V but T107BL is powered by VDD 3.3V.

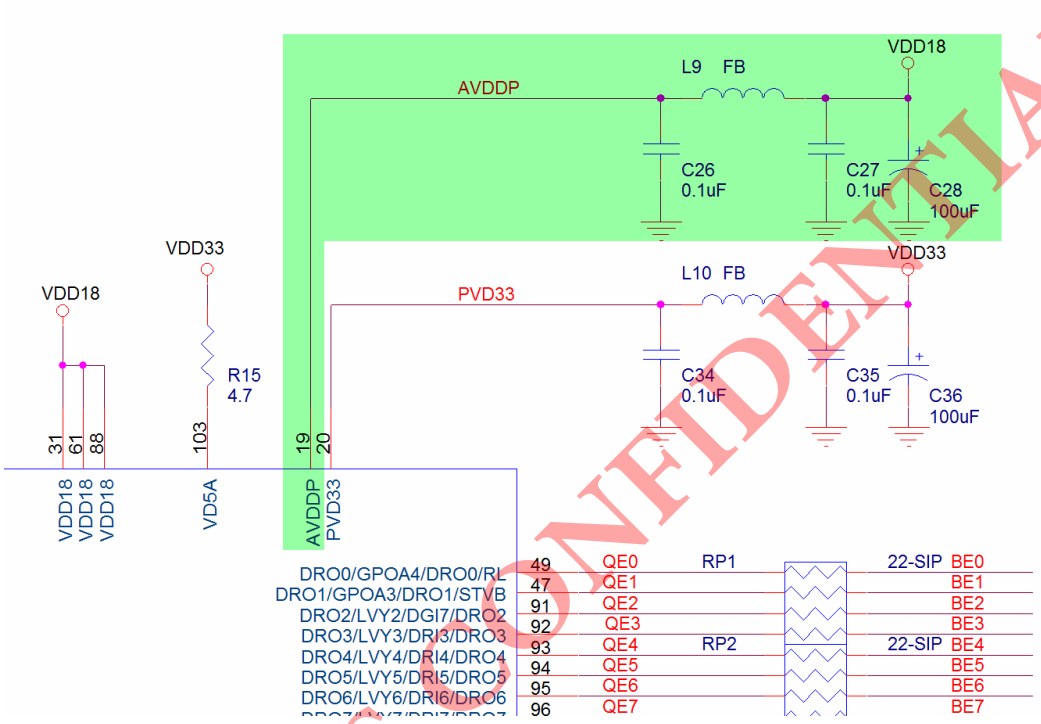

Figure 1-3 T107DL original AVDDP circuit.

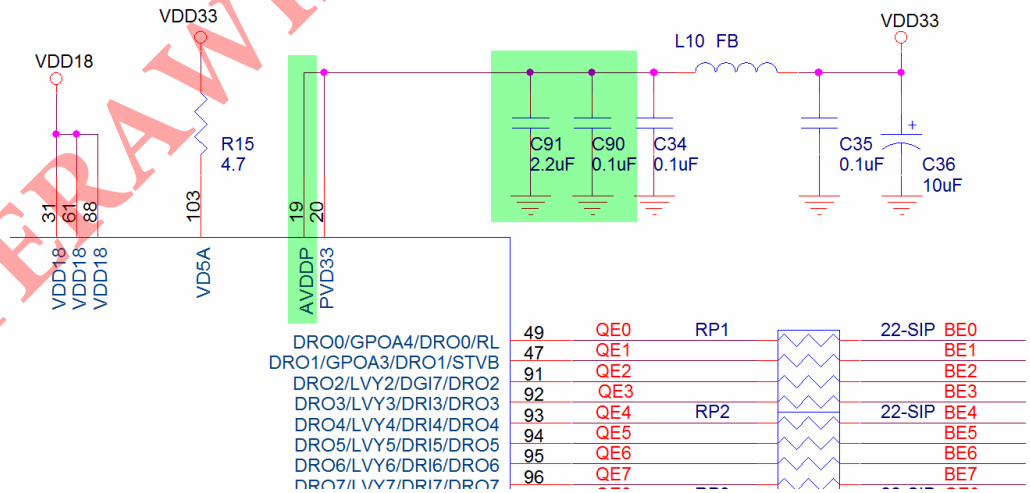

Figure 1-4 T107BL new AVDDP circuit.

1.2.2 DC-to-DC converter circuit

Remove (NC) all components used in CSS, CEXT, VEA and VISen of T107DL(C60, C61, C62, R61, R72 and R74 in Fig. 1-5). T107BL's pin assignment is the same as T107DL, so you could apply the original T107DL's schematics/PCB directly and let above components NC(but R74 should be 0ohm or short to GND).

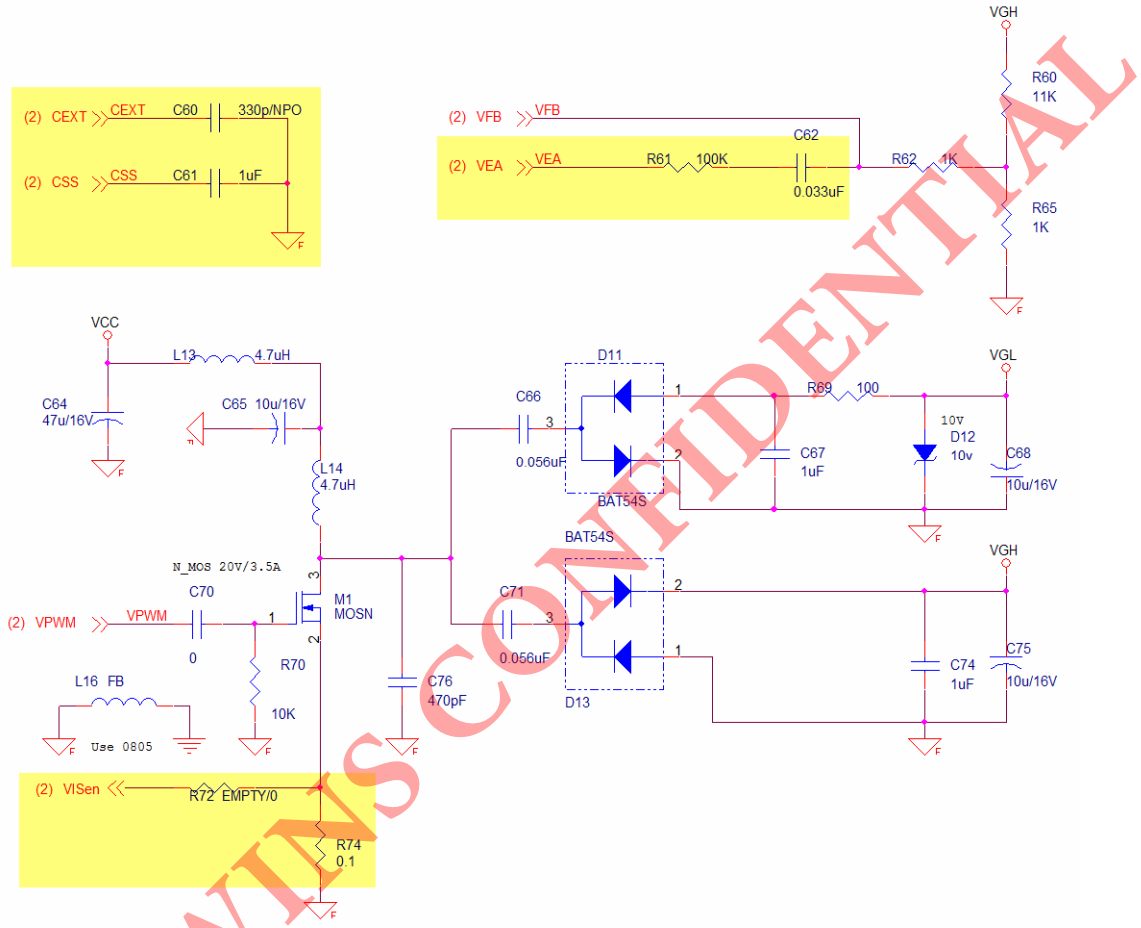

Figure 1-5 T107DL's original DC-to-DC converter circuit.

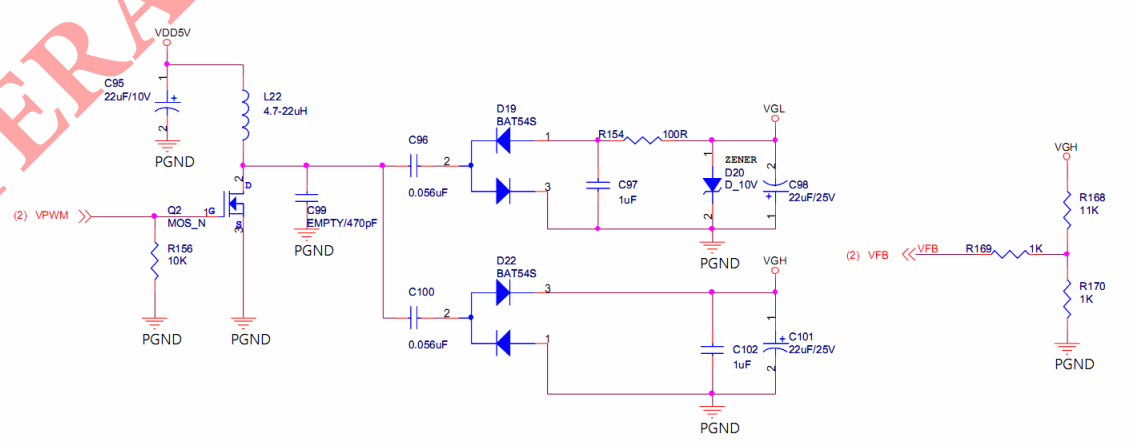

Figure 1-6 T107BL's new DC-to-DC converter circuit.

1.2.3 LED backlight control circuit

Remove (NC) all components used in CSSL, CEXTL, VEAL and VISenL of T107DL(C63, C77, C78, R67, R73 and R75 in Fig. 1-7) and add C103 and R174 to the VFBL trace of T107BL. T107BL's pin assignment is the same as T107DL, so you could apply the original T107DL's schematics/PCB directly and let above components NC(but R75 should be 0ohm or short to GND).

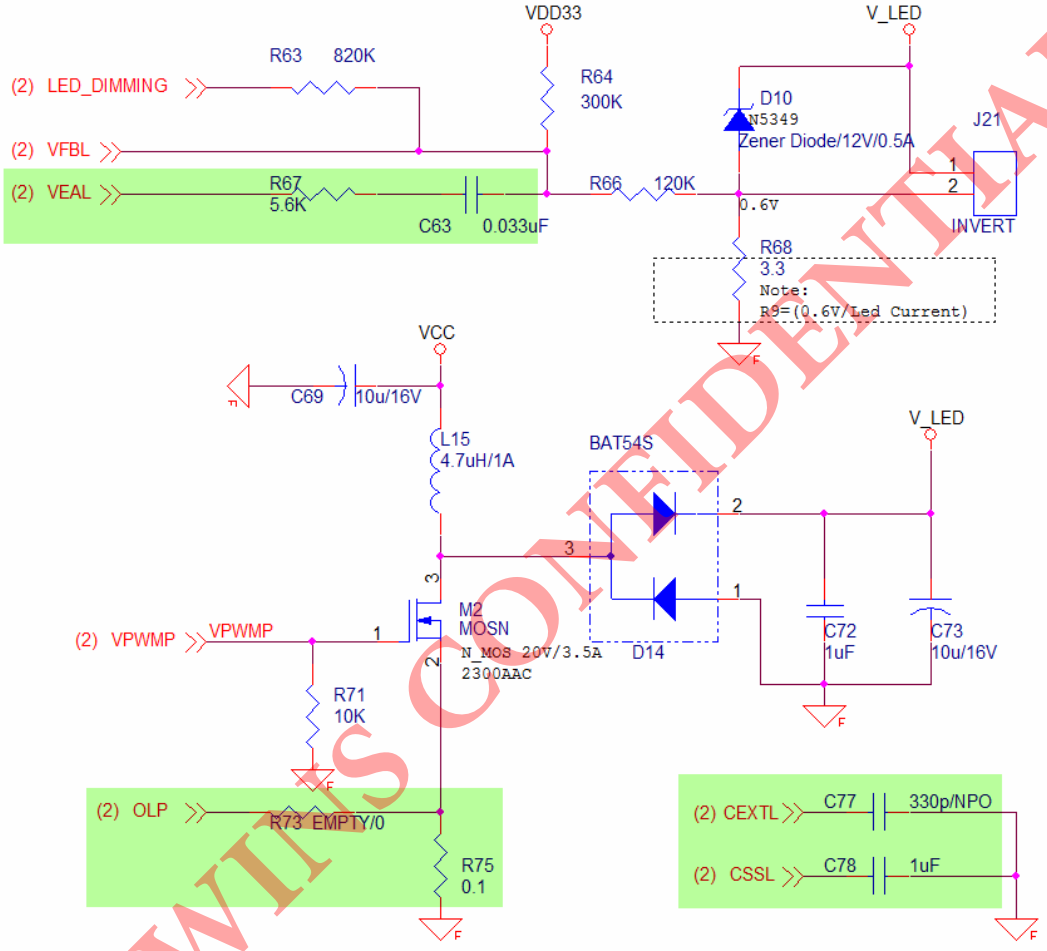

Figure 1-7 T107DL's LED backlight control circuit.

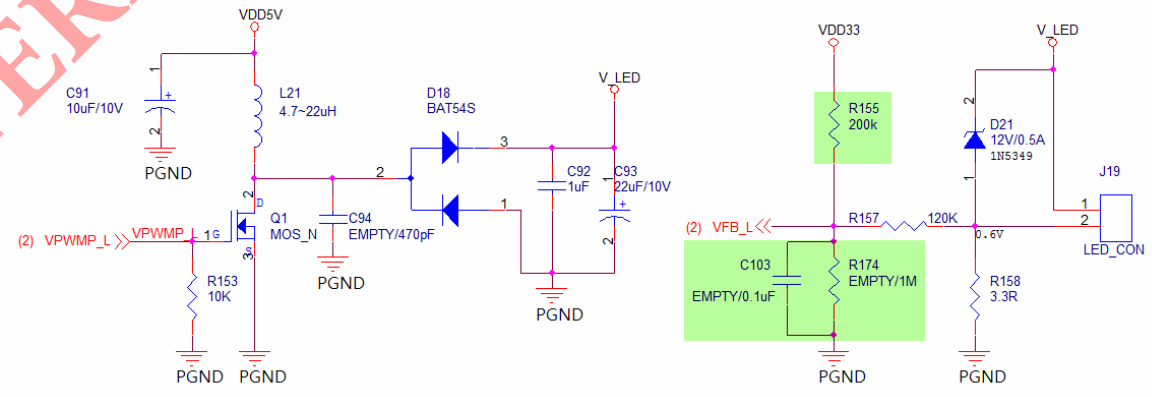

Figure 1-7 T107BL's LED backlight control circuit.

1.2.4 LPLL filter circuit for VGA input

Original LPLL filter circuit for T107DL is shown as Fig. 1-8, its reference point is VPLL and changed to ground for T107BL as shown in Fig. 1-9. The values of the filter components are also changed as C37 to 3300p, C40 to 330p and R22 to 15K Ohm.

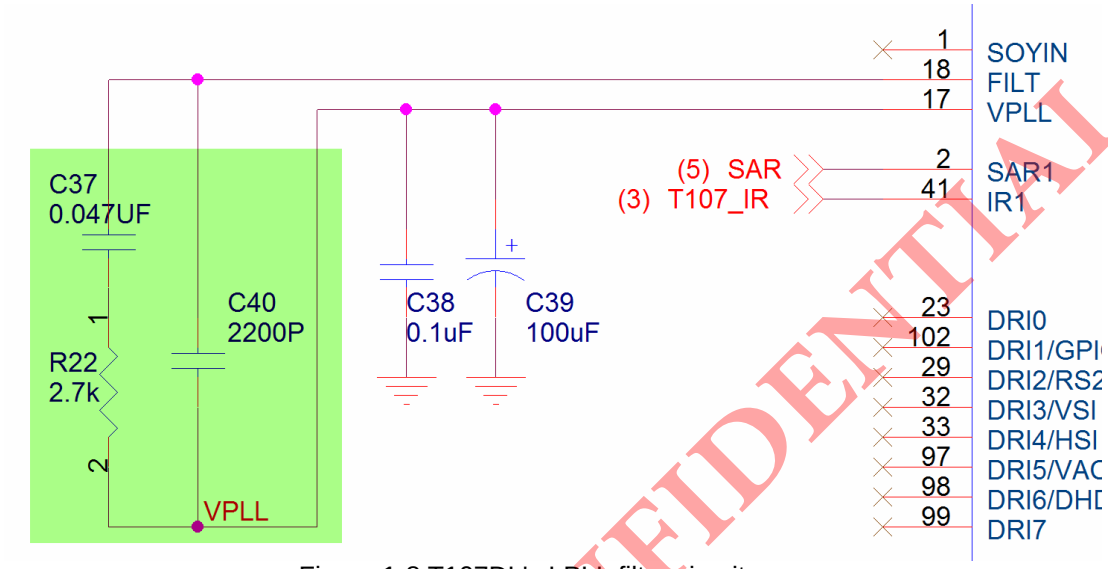

Figure 1-8 T107DL's LPLL filter circuit.

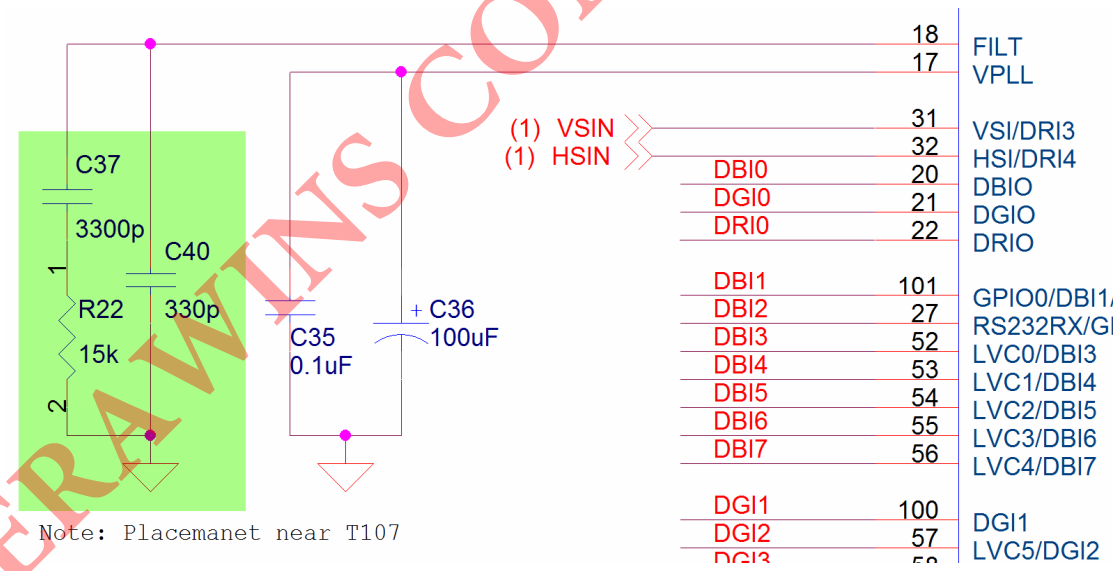

Figure 1-9 T107BL's LPLL filter circuit.

1.3 Firmware Control Differences

1.3.1 DC-to-DC controller

1.3.1.1 Relative control registers

➢DAC Power Management

Address Offset: P0_E3h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PDn_Bias	1: power down Bias circuit 0: power on Bias circuit
[6]	R/W	PDn_VCOM	1: power down Analog VCOM Amp circuit 0: power on Analog VCOM Amp circuit
[5]	RO	Reserved	
[4]	R/W	PDn_DC2DC_	1: power on DC to DC circuit 0: power down DC to DC circuit
[3]	R/W	SL	1: power down 3 channels 0: power on 3 channels
[2]	R/W	SLR	1: power down R channel 0: power on R channel
[1]	R/W	SLG	1: power down G channel 0: power on G channel
[0]	R/W	SLB	1: power down B channel 0: power on B channel

➢PWM23 Limit Register - 1

Address Offset: P1_60h Access: Read/Write
Default Value: 02h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	CCFL_Half_Bridge	1:Half bridge output; 0: Full bridge output
[6:4]	RO	Reserved	
[3:0]	R/W	PWM2_DeadTimer_sel	When PWM2_DeadTimer[2:1]==00b, shutdown immediately 01h~0Fh : 2T/4T/6T/8T/…/30T

➢PWM2 Control Register

Address Offset: P1_62h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PWM2_En	Enable PWM2
[6]	R/W	PWM2_Track	0b: Assign mode, 1b: Track mode;
[5:4]	R/W	PWM2_Freq_Sel	00b~11b: divided 1/2/4/8
[3:2]	R/W	PWM2_Step_Sel	00b~11b: slower -> faster tracking
[1]	R/W	PWM2_FTClk_en	Enable Fractional Fine Tune
[0]	R/W	PWM2_4bits_mode	Enable 4 bits mode, 0b: 1 bit, 1b: 4 bit

➢PWM2 Duty Register

Address Offset: P1_63h Access: Read/Write
Default Value: 10h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_High[7:0]	00~FFh means 1/PWM2_Period ~ 256/PWM2_Period; PWM2_En=0 means 0/PWM2_Period;

➢PWM2 Period Register

Address Offset: P1_64h Access: Read/Write
Default Value: 00h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_Period[7:0]	00h = 256T PWM2 frequency = Xtal (27MHz) / PWM2_Period

➢PWM2 & CCFL Control Register

Address Offset: P1_68h Access: Read/Write
Default Value: 06h Size: 8 bits

Bit	Access	Symbol	Description
[7]	R/W	PWM3_for_CCFL	Backlight control type: 1b: CCFL; 0b: LED
[6]	R/W	CCFL_ShD_to_Z	Shutdown control option
[5]	R/W	PWM23_Rd_Track	P1_63h/66h read back value as: 1b:tracked value; 0b:programmed PWM2/3_High[7:0]
[4]	R/W	PWM23_ShutDn_En	Enable over current protection
[3:2]	R/W	PWM3_TurnAround	CCFL full bridge skew
[1:0]	R/W	PWM23_Tip_Ahead	

➢PWM2 Range Register - 1

Address Offset: P1_69h Access: Read/Write
Default Value: 08h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_High_Min	Lower limit of PWM2 duty

➢PWM2 Range Register - 2

Address Offset: P1_6Ah Access: Read/Write
Default Value: 60h Size: 8 bits

Bit	Access	Symbol	Description
[7:0]	R/W	PWM2_High_Max	Upper limit of PWM2 duty

➢PWM Tip Selection

Address Offset: P1_7Fh Access: Read/Write
Default Value: 44h Size: 8 bits

Bit	Access	Symbol	Description
[7]	RO	Reserved	
[6:4]	R/W	PWM2_Tip_Sel	000b~111b: divided by 2^4~2^11
[3]	RO	Reserved	
[2:0]	R/W	PWM3_Tip_Sel	000b~111b: divided by 2^4~2^11

1.3.1.2 Control Sequence

I. Set the DPWM2 frequency, P1_64h; by default, frequency = 27Mhz / 256 ~= 105.5KHz.
II. Set the lower(P1_69h) & upper(P1_6Ah) limit duty and enable the protection(P1_68h[4] = 1b). While the **tracking duty > upper limit and standing > DeadTimer**(P1_60h[3:0]), the DPWM2 will be shut down for protection.
III. Set the tracking tip selection (P1_7Fh[6:4]). It is the time latency from DPWM output to VFB feedback. This value will be varied according to the application circuit.
IV.
V. Turn on the power of the controller block, P0_E3h[4] = 1b.
VI. Enable the DPWM output and the tracking (close loop), P1_62h = C0h

For example, the control sequence in the firmware would be similar to the following:

```
I2CWriteByte(T107_P1, 64h, 00h);
I2CWriteByte(T107_P1, 68h, 16h);
I2CWriteByte(T107_P1, 69h, 0Dh);
I2CWriteByte(T107_P1, 6Ah, 30h);
I2CWriteByte(T107_P1, 60h, 02h);
I2CWriteByte(T107_P1, 7Fh, 47h);
I2CWriteByte(T107_P0, E3h, 10h);
I2CWriteByte(T107_P1, 62h, C0h);
```

1.3.2 LED Backlight Controller

The LED backlight controller sequence is similar to DC-to-DC controller.

2 Revisions Note

Table 2-1 Revision Note

Revisions	Description of changes	Date	Note
1.00	First release	March 31, 2009	
1.01	Add pin 37 change description	June 1, 2009	

3 General Disclaimer

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